WHAT IS CLAIMED IS:

1. A method for effecting synchronous pulse generation for use in variable speed serial communications, comprising the steps of:

obtaining a communication link speed;

generating a difference signal representing a signal level difference between at least two data stream signals;

providing a clock signal;

providing a counter;

calculating a sample count value of said counter using said communication link speed;

incrementing said counter in relation to said clock signal;

determining whether a current count value of said counter corresponds to said sample count value, and

if said current count value corresponds to said sample count value then performing a step of generating a synchronous pulse, and

if said current count value does not correspond to said sample count value then performing a step of determining whether a signal level of said difference signal has changed, and if said signal level of said difference signal has changed then performing a step of ignoring further changes in said signal level of said difference signal until said current count value of said counter corresponds to said sample count value at which time said step of generating said synchronous pulse is repeated.

2. The method of claim 1, wherein said synchronous pulse is used to signify a time for performing a step of sampling said difference signal to extract data from said difference signal.

3. The method of claim 1, further comprising a step of defining a maximum count value of said counter, wherein if said current count value corresponds to said maximum count value then performing a step of resetting said counter.

4. The method of claim 1, wherein said step of determining whether said signal level of said difference signal has changed comprises the steps of:

checking said signal level of said difference signal each cycle of said clock signal;

storing said signal level of said difference signal at a first clock cycle as a temporary difference signal;

checking said signal level of said difference signal at a second clock cycle; and

comparing said signal level of said temporary difference signal with said signal level of said difference signal at said second clock cycle.

5. The method of claim 1, wherein said step of ignoring further changes in said signal level of said difference signal further comprises the steps of:

resetting said counter;

determining whether said current count value corresponds to said sample count value; and

if said current count value does not correspond to said sample count value then performing a step of incrementing said counter each cycle of said clock signal until said current count value corresponds to said sample count value at which time a step of sampling said difference signal to extract data from said difference signal is performed.

6. The method of claim 1, wherein a communication link with which said communication link speed is associated is an IEEE-1394b bus.

7. The method of claim 1, wherein said communication link speed is a frequency of one of 98.304 MHz, 196.608 MHz, 393.216 MHz, 786.432 MHz, 1.572864 GHz and 3.145728 GHz.

8. The method of claim 1, further comprising the step of identifying said communication link speed from a plurality of possible communication link speeds.

9. The method of claim 8, wherein said plurality of possible communication link speeds is greater than two.

10. A method of extracting data from a difference signal representing a signal level difference between two data stream signals, comprising the steps of:

providing a clock signal;

determining a communication link speed;

providing a counter;

defining a sample count value of said counter utilizing said communication link speed;

incrementing said counter in relation to said clock signal;

determining whether a current count value of said counter corresponds to said sample count value, and

if said current count value corresponds to said sample count value then performing a step of sampling said difference signal to extract data from said difference signal, and

if said current count value does not correspond to said sample count value then performing a step of determining whether a signal level of said difference signal has changed, and if said signal level of said difference signal has changed then performing a step of ignoring further changes in said signal level of said difference signal until said current count value of said counter corresponds to said sample count value at which time said step of sampling said difference signal to extract data from said difference signal is repeated.

11. The method of claim 10, wherein when said current count value corresponds to said sample count value, said method further comprises the step of generating a synchronization pulse to signify a time for said sampling of said difference signal to extract data from said difference signal.

12. The method of claim 10, wherein a communication link with which said communication link speed is associated is an IEEE-1349b bus.

13. The method of claim 10, wherein said communication link speed is a frequency of one of 98.304 MHz, 196.608 MHz, 393.216 MHz, 786.432 MHz, 1.572864 GHz and 3.145728 GHz.

14. The method of claim 10, further comprising the step of identifying said communication link speed from a plurality of possible communication link speeds.

15. The method of claim 14, wherein said plurality of possible communication link speeds is greater than two.

16. The method of claim 10, further comprising a step of defining a maximum count value of said counter, wherein if said current count value corresponds to said maximum count value then performing a step of resetting said counter.

17. The method of claim 10, wherein said step of determining whether said signal level of said difference signal has changed comprises the steps of:

checking said signal level of said difference signal each cycle of said clock signal;

storing a first signal level of said difference signal at a first clock cycle as a temporary difference signal;

checking a second signal level of said difference signal at a second clock cycle; and

comparing said first signal level of said temporary difference signal to said second signal level of said difference signal at said second clock cycle.

18. The method of claim 10, wherein said step of ignoring further changes in said signal level of said difference signal further comprises the steps of:

resetting said counter;

determining whether said current count value corresponds to said sample count value; and

if said current count value does not correspond to said sample count value then performing a step of incrementing said counter each cycle of said clock signal until said current count value corresponds to said sample count value at which time said step of sampling said difference signal to extract data from said difference signal is repeated.

19. A variable speed communications device, comprising:

a receiver having a first input, a second input and a first output, said first input being adapted for receiving a first data signal stream and said second input being adapted for receiving a second data signal stream, wherein said receiver processes said first data signal stream and said second data signal stream to generate a difference signal representing a difference between said first data signal stream and said second data signal stream; and

a synchronous pulse generator having a first difference signal input, a clock signal input, a speed input and a synchronous pulse output, said difference signal input being coupled to said first output for receiving said difference signal, said speed input being adapted to receive a variable representative of a communication link speed and said clock signal input being adapted for receiving a clock signal, wherein said synchronous pulse generator processes said clock signal, said communication link speed and said difference signal to generate a synchronous pulse used for extracting data from said difference signal.

20. The variable speed communications device of claim 19, further comprising:

a serial/parallel translator having a second difference signal input, a synchronous pulse input and an encoded data output, said second difference signal input being connected to said first difference signal input for receiving said difference signal and said synchronous pulse input being connected to said synchronous pulse output for receiving said synchronous pulse, and said serial/parallel translator processing said difference signal and said synchronous pulse to generate encoded data, said encoded data being output on said encoded data output;

an 8B/10B decoder having a third clock input, an encoded data input and a scrambled data output, said third clock input being coupled to said first clock input for receiving said clock signal, said encoded data input being coupled to said encoded data output for receiving said encoded data, wherein said 8B/10B decoder processes said clock signal and said encoded data to generate scrambled data for output on said scrambled data output; and

a descrambler having a fourth clock input, a scrambled data input and a parallel data output, said fourth clock input being coupled to said first clock input for receiving said clock signal, said scrambled data input being coupled to said scrambled data output for receiving said scrambled data, wherein said descrambler processes said clock signal and said scrambled data to generate parallel data for output on said parallel data output.

21. The variable speed communications device of claim 20, further comprising a packet receiver/transmitter having a parallel input, said parallel input being coupled to said parallel output of said descrambler for receiving said parallel data.

22. The variable speed communications device of claim 19, wherein said synchronous pulse generator includes a speed register for storing a speed value that corresponds with a communication speed of a serial bus.

23. The variable speed communications device of claim 22, wherein said speed value of said serial bus corresponds to a frequency of one of 98.304 MHz, 196.608 MHz, 393.216 MHz, 786.432 MHz, 1.572864 GHz and 3.145728 GHz.

24. An IEEE 1394b communications device, comprising:

a receiver having a first input, a second input and a first output, said first input being adapted for receiving a first data signal stream and said second input being adapted for receiving a second data stream, wherein said receiver processes said first data signal stream and said second data signal stream to generate a difference signal representing a difference between said first data signal stream and said second data signal stream;

a synchronous pulse generator having a first clock input, a first difference signal input, a speed input and a synchronous pulse output, said first clock input being adapted for receiving a clock signal, said speed input being adapted to receive a communication speed and said first difference signal input being coupled to said output for receiving said difference signal, wherein said synchronous pulse generator

processes said clock signal and said difference signal to generate a synchronous pulse used for extracting data from said difference signal;

a serial/parallel translator having a second clock input, a second difference signal input, a synchronous pulse input and an encoded data output, said second clock input being coupled to said first clock input for receiving said clock signal, said second difference signal input being connected to said first difference signal input for receiving said difference signal and said synchronous pulse input being connected to said synchronous pulse output for receiving said synchronous pulse, wherein said serial/parallel translator processes said clock signal, said difference signal and said synchronous pulse to generate encoded data for output on said encoded data output;

an 8B/10B decoder having a third clock input, an encoded data input and a scrambled data output, said third clock input being coupled to said first clock input for receiving said clock signal, said encoded data input being coupled to said encoded data output for receiving said encoded data, wherein said 8B/10B decoder processes said clock signal and said encoded data to generate scrambled data for output on said scrambled data output; and

a descrambler having a fourth clock input, a scrambled data input and a parallel data output, said fourth clock input being coupled to said first clock input for receiving said clock signal, said scrambled data input being coupled to said scrambled data output for receiving said scrambled data, wherein said descrambler processes said clock signal and said scrambled data to generate parallel data for output on said parallel data output.

25. The IEEE-1394b communications device of claim 24, further comprising a connection manager having a toning input, a toning output and a bus speed output; said toning input being adapted for receiving toning signals; said toning output being adapted for sending toning signals; said bus speed output being coupled to said speed input for providing said communication speed, wherein said connection manager processes said toning signals received on said toning input and sends toning signals on said toning output to establish said communication speed, and wherein said connection manager provides said communication speed to said bus speed output.

26. The IEEE-1394b communications device of claim 24, wherein said synchronous pulse generator includes a speed register for storing a speed value which corresponds with said communication speed.

27. The IEEE-1394b communications device of claim 26, wherein said communication speed is one of a frequency of 98.304 MHz, 196.608 MHz, 393.216 MHz, 786.432 MHz, 1.572864 GHz and 3.145728 GHz.

28. A method for synchronizing a receiver to data, comprising the steps of:
detecting a data speed;
initializing a counter to count clock cycles;
detecting a current count value;
defining a sampling count value based on said data speed;
detecting a change in said data;
incrementing said count value if no change in said data is detected; and,
generating a pulse when said counter reaches said sampling count value.

29. The method of claim 28, wherein said generating step occurs if a change in said data is detected.

30. The method of claim 28, wherein said generating step occurs when said count value equals said sampling count value.

31. The method of claim 28, further comprising the step of delaying said pulse to center said pulse in a data bit.

32. The method of claim 28, further comprising the step of resetting said current count value to zero when said pulse is generated.